Hybrid CMOS-SET Arithmetic Circuit Design Using Coulomb Blockade Oscillation Characteristic

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Hybrid CMOS-SET architectures, which combine the merits of CMOS and single electron transistor (SET) devices, promise to be a practical implementation for nanometer scale circuit design. In this work, we propose the design of two typical arithmetic circuits, namely adder and multiplier, using hybrid CMOS-SET architectures. For full adders (FAs) design, we present three different implementations based on multiple-valued logic (MVL), phase modulation and frequency modulation. These FAs fully utilize SET's unique characteristic of Coulomb blockade oscillation and exhibit improved performance in terms of circuit area/complexity, power dissipation and temperature effect. The structure based on frequency modulation also possesses high immunity against background charges, and is extended to design of multiple-bit adder and multiplier.

Keywords: Hybrid, Single Electron Transistor (SET), Multiple-Valued Logic (MVL), Modulation, Coulomb Blockade Oscillation, Power Dissipation, Background Charges.

1. INTRODUCTION

The scale-down of CMOS technology will inevitably hit the point where the quantum mechanical effect becomes predominant and hence makes it impossible to further shrink MOSFET dimensions.1 One possible candidate for next generation electronics is single-electron-tunneling technology.2 As one of the most sophisticated single electron devices (SED), single electron transistor (SET) is expected to be quite promising for future VLSI design due to its nanoscale feature-size, ultra low power dissipation and unique characteristic of Coulomb blockade oscillation.3 Circuits with SETs are also able to achieve a lot of new functionalities with less number of devices through novel design methodologies. However, pure SET-based circuits have very limited applications due to SET’s low current drivability, small voltage gain and extremely low-temperature operation.4 Since CMOS devices have advantages that can compensate for the intrinsic drawbacks of SET, hybrid CMOS-SET architecture which combines the merits of both CMOS and SET devices promises to be a much practical implementation for nanometer-scale circuit design.5

Full adder (FA) and multiplier are key elements for arithmetic operation. It is therefore of special interest to design these arithmetic circuits with extremely small size and ultra-low power dissipation. Extensive research work has been done on full adder design with SET technology, utilizing a variety of logic such as majority gate (MAJ),6,7 threshold logic gate (TLG),8 pass-transistor logic (PTL),9 binary decision diagram (BDD),10 and many others.11–14 While these pure SED-based adders dramatically reduce circuit area and power dissipation, they can only work at extremely low temperature (less than 10 K) due to the crucial limitation of thermal effect, making them impractical for real applications. Several FAs using hybrid CMOS-SET architecture have also been reported recently with increased temperature operation (up to room temperature).15–19 However, many of them15–17 simply adopted conventional CMOS structures which did not adequately take advantage of new characteristics of SETs. Some hybrid FAs18,19 did utilize Coulomb blockade oscillation characteristic that further reduces the number of devices, the less regularity of these circuits made them not suitable for VLSI design. Also, the background charge effect is a critical issue on circuit reliability, which has not been taken into account in the above FAs. Since multiplication can generally be viewed as repeated shifts and adds, multipliers can, in principle, be implemented easily in CMOS technology using only adders, shift registers and a certain amount of control logic. However, to the best of our knowledge, there is little research on multiplier design based on SET devices for significant improvement in both circuit area and power dissipation.

In this work, we propose three different implementations for hybrid CMOS-SET FAs by using multiple-valued logic (MVL), phase modulation and frequency modulation, with the goal of improving circuit area and complexity,
power dissipation and temperature effects. In particular, it is found that the structure based on frequency modulation shows high immunity against background charges, and is hence utilized to implement multiple-bit adders and multiplyers as well. Throughout the work, MIB (named after authors in) analytical model is used for SETs and all simulations are conducted using conventional SPICE simulator in Cadence at room temperature.21

2. BACKGROUND

SET is made of two tunnel junctions that share a common electrode, known as the island, with capacitively coupled gate terminals. A tunnel junction consists of two pieces of metal separated by a very thin (\textasciitilde 1 nm) insulator.3 According to the laws of classical electromagnetism, no current can flow through an insulating barrier. From the viewpoint of quantum mechanics, however, there is a non-vanishing probability for electrons to pass through the tunnel junction. Based on the orthodox theory which provides the unique guiding rules in single electrons;2 the tunneling of single electron through a tunnel junction is always a random event with a certain rate (also known as the tunneling rate) that depends solely on the reduction of free energy of the system as a result of this tunneling event.3 Therefore, from the microscopic point of view, the electron tunneling event is a stochastic process. From the macroscopic perspective, the current flowing through a tunnel junction is a deterministic behavior which depends on different external voltage or current biasing conditions.

For voltage/current biased SETs, the output drain current/voltage of SET exhibits an oscillating characteristic with respect to SET’s input gate voltage. This phenomenon is known as Coulomb blockade oscillation. It is well understood that the amplitude and period of the oscillation curve are inversely proportional to $C_C$ (i.e., the total capacitance on the island of SET with respect to the ground) and $C_G$ (i.e., the input gate capacitance), respectively. The phase of oscillation curve can be adjusted by the voltage applied on SET’s second gate with no effects on its amplitude and period. For the Coulomb blockade oscillation to occur, two criteria must be satisfied:

1. SET’s drain-to-source voltage (i.e., $V_{DS-SET}$) should be less than $3e/2C_C$. It has been observed that if $e/2C_C < V_{DS-SET} < 3e/2C_C$, the Coulomb blockade region will disappear but the Coulomb oscillation remains. If $V_{DS-SET} > 3e/2C_C$, the Coulomb oscillation phenomenon vanishes out and SET functions as a regular resistor.
2. The operating temperature should be very low (typically no more than 10 K). At a higher temperature, the thermal energy will significantly affect the electron tunneling rate with the likelihood of making tunneling events out of control.

With hybrid CMOS-SET architecture, the sub-ambient temperature operation (i.e., $-150 \degree C \sim -50 \degree C$) can be realized, thanks to the large voltage gain of MOSFETs.4 If SET’s device dimensions are further reduced so that $C_C$ is at the range of several aF, hybrid CMOS-SET circuits will be able to work at room temperature. There are two widely used hybrid CMOS-SET architectures, as shown in Figures 1(a) and (b) (in the remainder of the paper, they are called serial SETMOS and parallel SETMOS, respectively), where $V_{GG}$ and $V_S$ are used to bias NMOS transistors to work at sub-threshold region and $V_{PC}$ (‘PC’ stands for phase control) is used to adjust the phase of voltage oscillation at $V_{DS-SET}$. Due to the constant current biasing for NMOS transistor, $V_{DS-SET}$ oscillation can be transferred and amplified to the output node (i.e., $V_{OUT}$). In order to keep $V_{DS-SET}$ less than $3e/2C_C$, the biasing current through SET should be at the range of several tens of nA, which makes the current drivability of serial SETMOS very small. However, with separate biasing currents in parallel SETMOS (the one used to bias NMOS transistor is at the range of several $\mu$A), a higher current drivability at the output can be achieved.

3. THREE IMPLEMENTATIONS OF 1-BIT HYBRID CMOS-SET FAs

3.1. Multiple-Valued Logic (MVL) Scheme

For a current biased SET, due to holes accumulation at SET’s drain terminal, electrons induced from the ground will tunnel through both source and drain junctions of SET via the island, leading to a tunneling current. At steady state, the tunneling current equals to SET’s biasing current, which means that the number of electrons which successfully pass through SET’s junctions equals to the number of holes accumulated at SET’s drain terminal per unit time. The excess number of accumulated holes during the transient response contributes to SET’s drain voltage. Since SET’s input gate voltage has the impact on electron tunneling rate, it also affects the net amount of holes at SET’s drain terminal (i.e., $V_{DS-SET}$) at the steady state. In other words, the SET can be considered as a tunable resistor whose resistance is controlled by the voltage applied on SET’s gate terminal.

Fig. 1. (a) Serial SETMOS and (b) parallel SETMOS.
Let us consider three SETs connected in parallel, as shown in Figure 2(a) where all three SETs are identical with the same second gate biasing voltage \( V_{PC} \). This structure is analogous to three parallel resistors. Through appropriate configuration, each SET reaches its minimum (or maximum) resistivity with its input gate voltage (i.e., \( V_{IN} \)) being logic ‘0’ (or ‘1’). As a result, if all three inputs are logic ‘0’, the total equivalent resistance (i.e., \( R_{eq} \)) of three SETs is minimal, and thus \( V_{DS-SET} \) reaches its minimum value. As the number of 1’s in the input increases, so do the values of \( R_{eq} \) and \( V_{DS-SET} \). With all three inputs being logic ‘1’, \( R_{eq} \) and \( V_{DS-SET} \) will reach their maximum values. More specifically, as shown in Figure 2(b), if one input voltage (say \( V_{IN-A} \)) increases from zero to a considerable value with two other inputs being:

1. both logic ‘0’,
2. logic ‘0’ for one and logic ‘1’ for the other, or
3. both logic ‘1’, one can observe three voltage oscillation curves at \( V_{DS-SET} \) which have the same period and phase but different voltage levels.

In terms of digital applications, six points (i.e., \( P_0 \sim P_5 \) in the figure) can be obtained from the three curves located at four different voltage levels (i.e., \( V_0 \sim V_3 \)) which represent eight input patterns (i.e., 000, 001, 111).

In order to realize Carry and Sum functions for the adder design, the four intermediate voltage values need to be properly re-allocated into two voltage levels. A parallel SETMOS can be used to realize such a voltage conversion. By adjusting the period and phase of \( V_{DS-SET} \) oscillation, the output voltage oscillation of parallel SETMOS can be configured to the pattern as shown in Figure 2(c), in order to generate Carry and Sum outputs. The overall schematic of 1-bit FA using the above MVL scheme is shown in Figure 2(d).

Parallel connected multiple-SET architecture can also be used to implement D/A converters. Since SET can be regarded as a voltage controlled tunable resistor, the equivalent resistance of all SETs and hence the corresponding voltage at \( V_{DS-SET} \) can be modulated to represent the value of digital inputs rather than the number of 1’s in the inputs as long as each individual SET is properly weighted.

### 3.2. Phase Modulation Scheme

Instead of applying the inputs on three SETs, one can use only one SET with multiple input gates to accommodate three input digits, as shown in Figure 3(a) where the three left-hand-side gates of SET are identical and used to accept three input digits, and the fourth right-hand-side gate of SET is used to adjust the phase of voltage oscillation at \( V_{DS-SET} \). This is known as phase modulation scheme. Unlike the MVL scheme which moves \( V_{DS-SET} \) oscillation vertically, the phase modulation scheme moves \( V_{DS-SET} \) oscillation horizontally based on different input patterns.

By adjusting the device capacitance of SET and biasing voltage \( V_{PC} \), the \( V_{DS-SET} \) oscillation (as a result of increasing one input) can be configured to the pattern as shown in Figure 3(b) where the axes \( Y_0, Y_1 \) and \( Y_2 \) correspond to the condition of two other inputs being:

1. both logic ‘0’,
2. logic ‘0’ for one and logic ‘1’ for the other, or
3. both logic ‘1’, respectively.

It is observed that eight input patterns (i.e., 000, 001, ..., 111) are well distributed at four points (i.e., \( P_0 \sim P_3 \)) on the oscillation curve. For the Sum function, a half-period phase shift occurs each time one input digit alters its logic value. For the Carry function, since the period is doubled, only one-fourth period phase shift is obtained under the
same operation. Both Carry and Sum outputs can be implemented using the same circuit architecture with different parameters.

3.3. Frequency Modulation Scheme

It should be noticed that the previous two schemes for FAs strongly depend on particular voltages at the operating point. They work properly with no background charges on SETs. However, with background charges which are random in nature and cannot be entirely removed by today’s technology,22 the above circuits may fail to function correctly, depending on the amount of charges. In order to construct a robust hybrid CMOS-SET FA against background charge fluctuation, we propose yet another scheme—frequency modulation scheme—as follows.

The circuit structure based on frequency modulation scheme is shown in Figure 4(a), where three left-hand-side gates of SET are identical and directly connected to three NMOS transistors that function as switches. The digital inputs are used to control NMOS switches (on or off). $V_s$ is a monotonically increase voltage applied via NMOS switches on SET’s input gate terminals. Due to the fact that the node capacitance between NMOS and SET devices is relatively large (at the range of several fF), SET’s input gate capacitance (at the range of several aF) in such a structure would not be affected by the NMOS devices. With $V_s$ applied on any of SET’s input gate terminals, the period of voltage oscillation at $V_{DS-SET}$ is inversely proportional to SET’s input gate capacitance. If the $V_s$ is applied on multiple input gates of SET, the period of $V_{DS-SET}$ oscillation is determined by the total capacitance of those gates connected with $V_s$. Since three input digits applied on NMOS switches are able to control the connection between $V_s$ and input gates of SET, the total input gate capacitance and hence the period of $V_{DS-SET}$ oscillation is defined by different input patterns. When $V_s$ increases from zero to $V_{TOP}$, as shown in Figure 4(b), the number of 1’s in the inputs is modulated into the number of voltage oscillation cycles at $V_{DS-SET}$.

Due to the high operating speed of SET, the oscillation at $V_{DS-SET}$ is reflected into the time domain. By using a 2-bit ripple counter, the number of voltage oscillation cycles at the output with respect to time is recorded in the binary system, and the counter’s outputs represent the Carry and Sum bits. As long as background charges on the island of SET keep constant during the period of varying $V_s$, the same number of voltage oscillation cycles will appear at the output. Since the amount of background charges on SET’s island varies at a relatively low frequency,22 the circuit will exhibit much higher immunity against background effect.

4. APPLICATIONS USING FREQUENCY MODULATION SCHEME

4.1. Multiple-Bit Full Adders

The frequency modulation scheme can also be used to implement multiple-bit FAs and multipliers. For the case of FAs, to accept higher-order input bits, one simply needs to add more input gates for the SET, which are connected via NMOS switches with $V_s$, and the higher-order output bits can be obtained by adding more cells for the ripple counter.

As an example, Figure 5(a) shows the overall schematic of 2-bit FA, where the input gate capacitances for $x1$ and $y1$ are twice as much as those for $x0$ and $y0$, and three D flip-flops are used to generate the three output bits. For $n$-bit FA in general, the SET will have $(2n+1)$ input gates.
whose capacitance corresponding to the $i$th (with $i$ starting from 1) input bit is $i$ times as much as that for the least significant input bit, and the number of $D$ flip-flops for the ripple counter is $n + 1$. Since each $D$ flip-flop can be implemented with minimum of 8 MOS transistors, the total number of MOS transistors needed is $(2n + 1) + 1 + 8n = 10n + 2$. With CMOS technology, $n$-bit ripple carry adder requires $24n$ MOS transistors, which is the minimum hardware required for $n$-bit FA. The $n$-bit hybrid CMOS-SET FA using frequency modulation scheme dramatically reduces the circuit area and power dissipation, especially for a large value of $n$ (the area and power consumed by SET device are negligible compared to CMOS devices).

4.2. Multiple-Bit Multipliers

In the structure based on frequency modulation scheme, the number of voltage oscillation cycles at the output is not only determined by the total input gate capacitance of SET, but also affected by the varying range of $V_s$. For instance, if the range of $V_s$ is two times greater, the number of voltage oscillation cycles will double. Therefore, by setting a maximum value of $V_s$ based on multiplicand (using a $D/A$ converter) and the total input gate capacitance based on multiplier, the number of voltage oscillation cycles at the output will represent the multiplication of the two operands.

Another method to realize multiplication is through a cascaded structure of parallel SETMOSs. It is understood that parallel SETMOS is able to generate voltage oscillation at the output by monotonically changing (either increasing or decreasing) $V_s$. If the $V_s$ is chosen to be a cycle (say, increasing from zero to a certain value then returning back to zero), as long as the dynamic ranges of input and output voltage are the same, each output voltage oscillation cycle can serve as the voltage $V_s$ for the next parallel SETMOS. Therefore, with two parallel SETMOSs connected in serial, where each of them is configured by an operand (whose value is assumed to be $N$) in such a way that one cycle of $V_s$ will generate $N$ cycles of output voltage, the number of voltage oscillation cycles at the output of the second parallel SETMOS will represent the multiplication of the two operands.

Figure 5(b) shows the overall schematic of 3-bit multiplier using the cascaded structure of two parallel SETMOSs, where the input gate capacitances of SET should be weighed properly for each operand. The circuit can also perform multiplication with multiple operands using multiple stages, and each stage can be designed to accept more than one operand (using the structure in Fig. 5(a)) so that the addition and multiplication operations can be performed simultaneously.

5. PARAMETER SELECTION OF THE PROPOSED CIRCUITS

All proposed hybrid CMOS-SET circuits share the same parameters of $R_{TD} = R_{TS} = 1 \text{ M}\Omega$ and $C_{TD} = C_{TS} = 0.1 \text{ aF}$
(SET’s source and drain junction resistance and capacitance), $I_{D1} = 40 \, \text{nA}$ (SET’s biasing current), $I_{D2} = 1 \, \text{uA}$ (biasing current for NMOS transistor), $V_{TH-NMOS} = 150\sim200 \, \text{mV}$ (threshold voltage of NMOS transistor), and $T = 300 \, \text{K}$ (operating temperature). Other parameters used in the structures of three FAs (i.e., in Figs. 2(d), 3(a) and 4(a)) are listed in Table I. Figure 6 shows the simulation result of MVL based FA using the provided parameters.

To simulate the circuit based on frequency modulation, extra control units are needed so that the ripple counter is initialized to zero each time before the evaluating operation (i.e., get the output by changing $V_s$). For multiple-bit adders and multipliers, as shown in Figures 5(a) and (b), $C_{G1}$ and $C_{G2}$ are the same as those used in FA based on frequency modulation but the values of $V_{PC}$ are different.

### 6. CONCLUSIONS

We have proposed three hybrid CMOS-SET full adders based on multiple-valued logic (MVL), phase modulation and frequency modulation. For the MVL scheme, SET is considered as a voltage controlled tunable resistor. This method can also be used to implement $D/A$ converters. For
the phase modulation scheme, the Carry and Sum functions are realized by changing the phase of voltage oscillation. In the frequency modulation scheme, the voltage oscillation is reflected in the time domain, and the output is generated by counting the number of oscillation cycles. With this method, a higher immunity against background charges is achieved when the circuit works at a relatively high frequency. The frequency modulation scheme has also been utilized easily to implement multiple-bit adders and multipliers.

Acknowledgments: This work was supported in part by the Natural Sciences and Engineering Research Council of Canada (NSERC).

References


Received: 21 September 2010. Accepted: 23 January 2011.